REMARKS

Claim 1 was rejected under 35 U.S.C. Section 103 as being unpatentable over Nishida et al. (U.S. Patent No. 3,789,503) in view of Liaw et al. (U.S. Patent No. 5,141,887). Applicants' Claim 1 recites: "An electrical semiconductor device comprising: a substrate of relatively high resistivity material of one conductivity type having opposing first and second surfaces, the first surface being etched; a layer of relatively low resistivity material of the one conductivity type and having one surface substantially contiguous to the first surface of the substrate; and an epitaxial region of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having one surface substantially contiguous to the second surface of the substrate." In marked contrast, FIG. 1 of Nishida et al. was cited for disclosing a substrate 11 of relatively high resistivity material with one conductivity type having opposing first and second surfaces and a **layer 14** of relatively low resistivity material of the **one conductivity type**. However, it is respectfully believed, that FIG. 1 of Nishida et al. clearly shows that layer 14 constitutes separate, diffuse regions that are N, N^+ and P^+, respectively. **It is not of one conductivity type.** Column 1, Lines 65-67 and Column 2, Lines 1-13 of Nishida et al. were also cited and recite: "This invention comprises the steps of forming a thin semiconductor layer of low resistivity and of the same conductivity type as the substrate by diffusing an impurity into a major substrate **excluding a gate portion** of a high resistivity silicon semiconductor substrate having one conductivity type, **selectively forming** an insulating film such as silicon oxide film on the substrate, **forming active regions** such as a source, a drain and a semiconductor region

for protecting the gate insulator through holes formed in the oxide film by diffusing an impurity of a conductivity type different from that of a substrate, forming a thin gate insulator by making a portion of the oxide film thin, selectively removing portions of the oxide film, and forming interconnections in ohmic contact with the respective semiconductor region." **Therefore, it is respectfully believed that a layer 14 of relatively low resistivity material of the one conductivity type is not disclosed in Nishiba et al. but merely selective and discrete regions of differing conductivity types.** It is respectfully believed that all claim limitations must be considered and a Reference that recites a collection of differing conductivity types, i.e., N, N^+ and P^+, will not render a claim limitation requiring a layer of relatively low resistivity material of one conductivity type obvious to one of ordinary skill in the art.

Liaw et al. is cited for "---teaching an epitaxial region of a conductivity type opposite to the one conductivity type and having one surface substantially contiguous to the second surface of the substrate." A select portion of Claim 29 of Liaw et al. is cited for support. The full recitation of Claim 29 is as follows: "A method of fabricating a deep junction device having a breakdown voltage of less than 20 volts, said method comprising the steps of: providing a first semiconductor wafer of a first conductivity type, said first wafer having a first surface, a second surface and a dopant concentration of at least 4.0×10^{16} atoms/cc; providing a second semiconductor wafer of a second conductivity type, said second wafer having a first surface, a second surface and a dopant concentration at least $4.0.x\ 10^{16}$ atoms/cc; removing impurities from said first and second wafers; bonding said first semiconductor surfaces of said first and second wafers directly together; and bonding an additional doped semiconductor wafer or forming a

semiconductor epitaxial layer on the second surface of one or both of said first and second wafers to create multiple junctions." Therefore, Liaw et al. discloses two separate semiconductor wafers that are bonded together and not one substrate having a layer on one side and an epitaxial region on the other side of the substrate.

It is respectfully believed that there must be some basis for combining or modifying the References. In this case, the layer 14 of Nishida et al. is a variety of variety of conductivity types and not one layer of one conductivity type. Liaw et al. only discloses the general proposition of epitaxial growth on two bonded semiconductor wafers. It does not disclose a substrate of relatively high resistivity material that is contiguous to a layer of low resistivity material on a first, **etched,** surface of the substrate and an epitaxial growth region on the second surface of the substrate. It is respectfully believed that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching, suggestion or incentive. In this case, there are no suggestions or teachings present and the combination of both Nishida et al. and Liaw et al. will not result in the Invention as recited in Applicants' Claim 1. It is now a basic tenet of patent law that the results and advantages produced by the claimed subject matter, of which the prior art is devoid, cannot be ignored simply because the claim limitations are similar to the otherwise barren prior art. It is respectfully believed that patentability of the claimed subject matter must be determined in view of the invention "as a whole".

It is also respectfully believed that it is not proper standard to try a modification and/or combination of references. In this case, it is not proper to modify layer 14 of Nishida et al. to a layer of single conductive type material from the variety of conductive type materials in layer 14

recited in that Patent without a hint or suggestion to make this modification.

Moreover, the recited claim limitation that the first surface of the substrate is etched is for the purpose of: "In a preferred embodiment, a photo-resist mask 18a is removably applied to the opposing surface of the epitaxial layer 16a. Exposed portions of the opposing surface of the epitaxial layer 16a are then **directly etched to a predetermined depth, forming a central cavity or well 20a in each exposed portion, each well 20a corresponding to an individual semiconductor device 22a.** Upon removal of the mask 18a, a high conductivity dopant region 24a is diffused into the opposing surface of the epitaxial layer 16a." (Applicants' Specification, Page 5, Lines 22-27). Therefore, this etching is to create specific types of semiconductor devices having particular characteristics. The concept of etching for "---removal of native oxides and contaminants accumulated during handling" would destroy the Applicants' Invention for its stated purpose since the etching must be exact to provide wells of a particular dimension for specific semiconductor properties. It is respectfully believed that to remove impurities without regard for the dimensions will result in inconsistent semiconductor devices that would not be commercially marketable since the dimensions and thus the properties of the semiconductor would not be consistent.

Moreover, not only are the claim limitations unique when contrasted to Nishida et al. and Liaw et al., but the Applicants' Invention, as claimed, solves a significant problem of providing protection to high reverse voltage semiconductor devices from high reverse voltages or reverse currents. It is respectfully believed ever since Eibel Process Co. v. Minnesota and Ontario Paper Co., 261 U.S. 45 (1923), that the U.S. Supreme Court, the Federal Court of Appeals for the

Federal Circuit as well as the United States Patent Office has recognized the longstanding rule that discovery of the source of the problem is patentable even if the solution is deemed obvious (which is not the present situation). In this case, the pitch of a paper-making mesh conveyor was altered to impart a component of gravity to the paper stock. Although it was known that altering the pitch of the paper-making mesh conveyor would alter the performance of the machine, it was deemed patentable to discover that the source of the problem, i.e., ripples in the paper stock, could be eliminated by altering the pitch of the paper-making mesh conveyor. In this situation, the etching of the substrate solves the significant problem of breakdown with high reverse voltage that would not be obvious to someone with ordinary skill based on etching of semiconductors performed for removing native oxides and contaminants.

Therefore, Claim 1 overcomes the rejection under 35 U.S.C. Section 103 as being unpatentable over Nishida et al. in view of Liaw et al.

Claim 2 was also rejected under 35 U.S.C. Section 103 as being unpatentable over Nishida et al. in view of Liaw et al. Since Claim 2 depends from and contain all of the limitations of Claim 1, Claim 2 is felt to distinguish from Nishida et al. in view of Liaw et al. in the same manner as Claim 1.

Claims 4 and 5 were rejected under 35 U.S.C. Section 103 as being unpatentable over Nishida et al in view of Liaw et al. as applied to Claims 1-2 above and further in view of Davis et al. (U. S. Patent No. 5,668,397). Since Claims 4 and 5 depend from and contain all of the limitations of Claim 1, Claims 4 and 5 are felt to distinguish from Nishida et al. in view of Liaw et al. in the same manner as Claim 1. Moreover, Davis et al. recites the use of impurities to:

"The heavily doped regions 14 and 16 are formed with high concentrations of boron and phosphorus. Since these species have smaller atomic radii than silicon, substantial lattice defects can extend from this region of the crystal structure. If permitted, such defects would cause significant **current leakage across junctions**, thereby **degrading analog performance characteristics** in the transistors." (Column 4, Lines 25-31). Therefore, the addition of stress relieving dopant in Davis et al. is to minimize leakage current in a low voltage CMOS device. There is no hint or suggestion as to why someone with ordinary skill in the art would combine Davis et al. with Nishida et al. and Liaw et al. since the presence of stress reliving dopant is to relieve stress in the epitaxial region in Applicants' claimed Invention is to prevent the entire substrate from cracking when high reverse voltage is present and not to minimize leakage current in a low voltage CMOS device. It is respectfully believed that what is obvious is only that which can be deduced by a logical step-by-step reasoning process from the premises furnished by the prior art. In this case, the use of a stress-relieving dopant, e.g., germanium, to is to relieve stress in the epitaxial region in Applicants' claimed Invention cannot be inferred from a cited Reference that uses impurities **to minimize leakage current in a low voltage CMOS device**.

Therefore, Claims 4 and 5 overcome the rejection under 35 U.S.C. Section 103 as being unpatentable over Nishida et al. in view of Liaw et al. as applied to Claims 1-2 above and further in view of Davis et al.

Claims 6, 12 and 21 were rejected under 35 U.S.C. Section 103 as being unpatentable over Nishida et al in view of Liaw et al. and further in view of Yamada (U. S. Patent No. 6,160,288). As previously stated, Nishida et al discloses a layer 14 that constitutes a variety of

conductivity types in separate, diffuse regions that are N, N^+ and P^+, respectively or as in FIG. 3(a) the two layers of the same conductivity type with different levels of doping. Nishida et al. does not disclose: "----an epitaxial layer of relatively high resistivity material of **one conductivity type** and having opposing first and second surfaces; a substrate of relatively low resistivity material of a conductivity type **opposite to the one conductivity type** and having a surface substantially contiguous to the first surface of the epitaxial layer." Also, Liaw et al., as previously discussed, requires the presence of two silicon wafers that are bonded together. There may a single epitaxial layer attached to one outer surface of one of the silicon wafers or two epitaxial layers with one epitaxial layer located on the outer surface of the first silicon wafer and another epitaxial layer located on the outer surface of the second silicon wafer.

Liaw et al. does not disclose an epitaxial layer of relatively high resistivity material of one conductivity type and having opposing first and second surfaces, a substrate of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having a surface substantially contiguous to the first surface of the epitaxial layer and a region of relatively low resistivity material of the one conductivity type having a surface substantially contiguous to the second surface of the epitaxial layer.

Yamada is cited for disclosing a substrate 1 and an epitaxial layer 2, as shown in FIG. 1. However, it is clear that FIG. 1 in Yamada, requires the substrate 1 to be of n^+ type material and the epitaxial layer 2 be of n^- type material. This is the same conductivity type with differing levels of doping and not the opposite conductivity type as required in Claims 6, 12 and 21. It is respectfully believed that all claim limitations must be considered and that there must be some

basis in the art for combining the above-cited References. It is believed to be axiomatic that a valid rejection under 35 U.S.C. Section 103 cannot be made when the combination of References still does not result in the Applicants' claimed Invention. While as an abstract proposition, it might be possible to select features from Yamada and Liaw et al., as the examiner has done and mechanically combine them with Nishida et al. to attempt to arrive at the Applicants' claimed Invention, there is absolutely not basis for making such combination neither disclosed nor suggested in the patents relied on. In our view, only the Applicants' specification suggests any reason for combining and modifying the features found in the cited References and, under the provisions of 35 U.S.C. Section 103, that does not constitute a bar.

Therefore, Claims 6, 12 and 21 overcome the rejection under 35 U.S.C. Section 103 as being unpatentable over Nishida et al. in view of Liaw et al. as applied to Claims 1-2 above and further in view of Yamada.

Claims 3, 7-9 and 15 were rejected under 35 U.S.C. Section 103 as being unpatentable over Nishida et al in view of Liaw et al. and further in view of Yamada. Since Claims 3, 7-8, and 15 depend from and contain all of the limitations of Claims 1, 6 and 12, Claims 3, 7-8, and 15 are felt to distinguish from Nishida et al. in view of Liaw et al. above and further in view of Yamada.

Claims 10-11 and 13-14 were rejected under 35 U.S.C. Section 103 as being unpatentable over Nishida et al in view of Liaw et al. and Yamada as applied to Claims 1-2 and Claims 4-5 above and further in view of Davis et al. Since Claims 10-11 depend from and contain all of the limitations of Claim 6, Claims 10-11 are felt to distinguish from Nishida et al. in view of Liaw et

al. and Yamada as applied to Claims 1-2 and Claims 4-5 above and further in view of Davis et al. in the same manner as Claim 6. Since Claims 13-14 depend from and contain all of the limitations of Claim 12, Claims 13-14 are felt to distinguish from Nishida et al. in view of Liaw et al. and Yamada as applied to Claims 1-2 and Claims 4-5 above and further in view of Davis et al. in the same manner as Claim 12.

Therefore, Claims 10-11 and 13-14 overcome the rejection under 35 U.S.C. Section 103 as being unpatentable over Nishida et al. in view of Liaw et al. and Yamada as applied to Claims 1-2 and Claims 4-5 further in view of Davis et al.

Claims 22-24 have been added to emphasize that the well 20 shown in FIGS. 3-9 reduces the amount of high resistivity material thereby reducing the electric field. Support for these Claims can be found on Page 1, Lines 32-33, Page 5, Lines 22-29, Page 6, Lines 11-13. This merely provides Applicants with entitled patent protection with no new matter being added.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

It is now believed that all of the pending claims in the present application, namely, claims 1-15 and 21-24 contain limitations and restrictions which patentably distinguish them over the cited prior art. None of the cited references, either alone or in any combination thereof, disclose or suggest all of the novel features associated with the present high reverse voltage semiconductor device as explained above, nor do the referenced constructions provide the

specific advantages and objectives obtained by the present device. Favorable action and allowance of the claims is therefore respectfully requested.

If any issue regarding the allowability of any of the pending claims in the present application could be readily resolved, or if other action could be taken to further advance this application such as an Examiner's amendment, or if the Examiner should have any questions regarding this amendment, it is respectfully requested that Examiner please telephone Applicants' undersigned attorney in this regard.

It is believed there is no fee due in regard to this amendment. However, any fees due in connection with this matter can be charged to our Deposit Account No. 11-0160.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please add the following Claims 22-24:

22. (New) The device of claim 2 wherein the etched first surface of the substrate forms a well that receives the diffused layer, wherein the diffused layer in the well reduces an area of the relatively high resistivity material in the substrate to reduce a resulting electric field.

23. (New) The device of claim 8 wherein the etched second surface of the epitaxial layer of relatively high resistivity material forms a well that reduces an area of the relatively high resistivity material in the second surface of the epitaxial layer of relatively high resistivity material to reduce a resulting electric field.

24. (New) The device of claim 15 wherein the second surface of the epitaxial layer of relatively high resistivity material receives a lesser amount of diffused material to form a well that reduces the area of the relatively high resistivity material in the second surface of the epitaxial layer of relatively high resistivity material to reduce a resulting electric field.